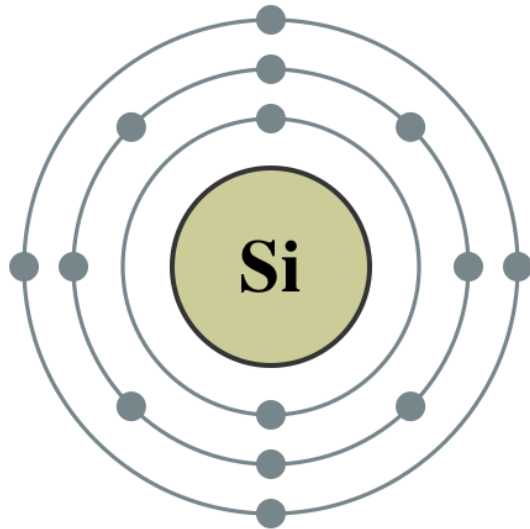


Digital PLL Design using XMODEL and Cell-Based Design Flow

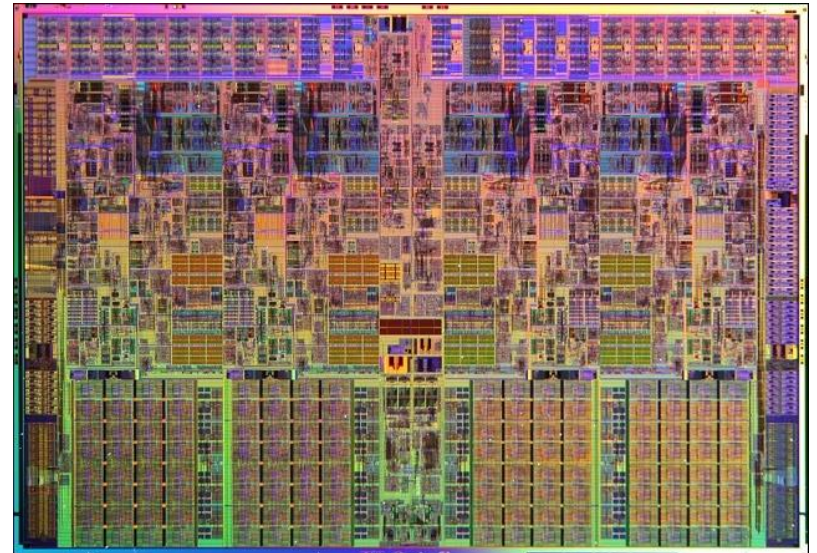
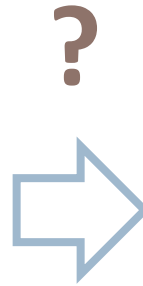
Jaeha Kim, Sung-Joon Lee, and Eunseo Kim
Mixed-Signal IC and System Group
Seoul National University
May 19. 2016

How Do We...

- ▶ Design a billion-transistor IC made of Si atoms?



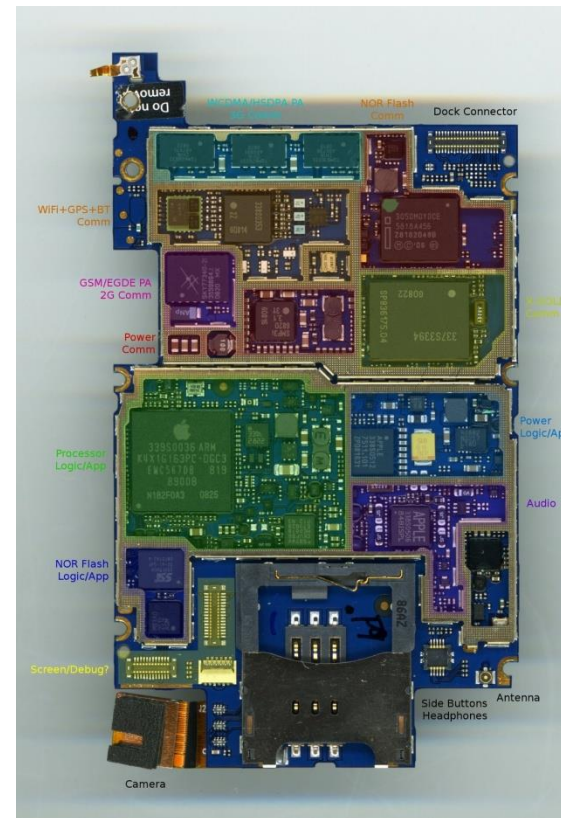
Silicon Atom



*Intel 4-core Nehalem
Processor*

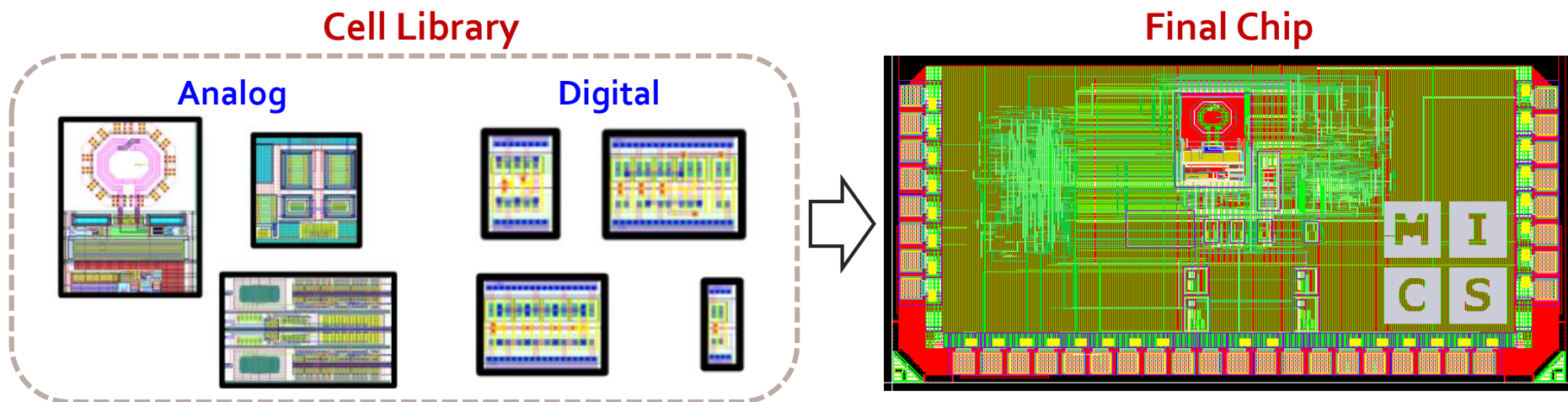
How Do We ... (2)

- And even build complex systems like smartphones?



Course Introduction

- ▶ **Cell-based design flow** for analog/mixed-signal system enables IC design and layout simply by putting ready-made cells together without technical knowledge of transistor-level circuit
- ▶ Learn how to use XMODEL and cell-based design flow for design, simulation, and layout of digital PLLs



Course Objectives

- ▶ Understanding cell-based design flow for mixed-signal system
- ▶ Digital phase-locked loop (PLL) design and simulation by Scientific Analog's XMODEL
- ▶ Digital PLL synthesis and place-and-route (P&R) utilizing Synopsys's Design Compiler and IC Compiler/Custom Designer

Course Schedules (Day 1)

▶ Morning

- ▶ Introduction to cell-based design flow
- ▶ Digital phase-locked loop (PLL) basics

▶ Afternoon

- ▶ Getting started with XMODEL
- ▶ Design and simulation of digital PLL using XMODEL
- ▶ Digital loop-filter synthesis using Design Compiler

Course Schedules (Day 2)

► Morning

- Introduction to IC Compiler/Customer Designer (ICCD) flow
- P&R practice (placement ~ decap insertion)

► Afternoon

- P&R practice (power rail & clock-tree synthesis ~ chip completion)
- Final DRC & LVS check

Teaching Staffs

- ▶ Main instructors:

- ▶ Sung-Joon Lee, MS candidate (sjlee@mics.snu.ac.kr)
- ▶ Eunseo Kim, MS candidate (eunseo@mics.snu.ac.kr)

- ▶ Supervising instructor: Prof. Jaeha Kim

- ▶ Associate Professor at Seoul National Univ. (SNU)
- ▶ CEO and Founder of Scientific Analog, Inc.
- ▶ BS from SNU and MS/PhD from Stanford Univ.
- ▶ Mixed-signal IC design and methodologies

Acknowledgements

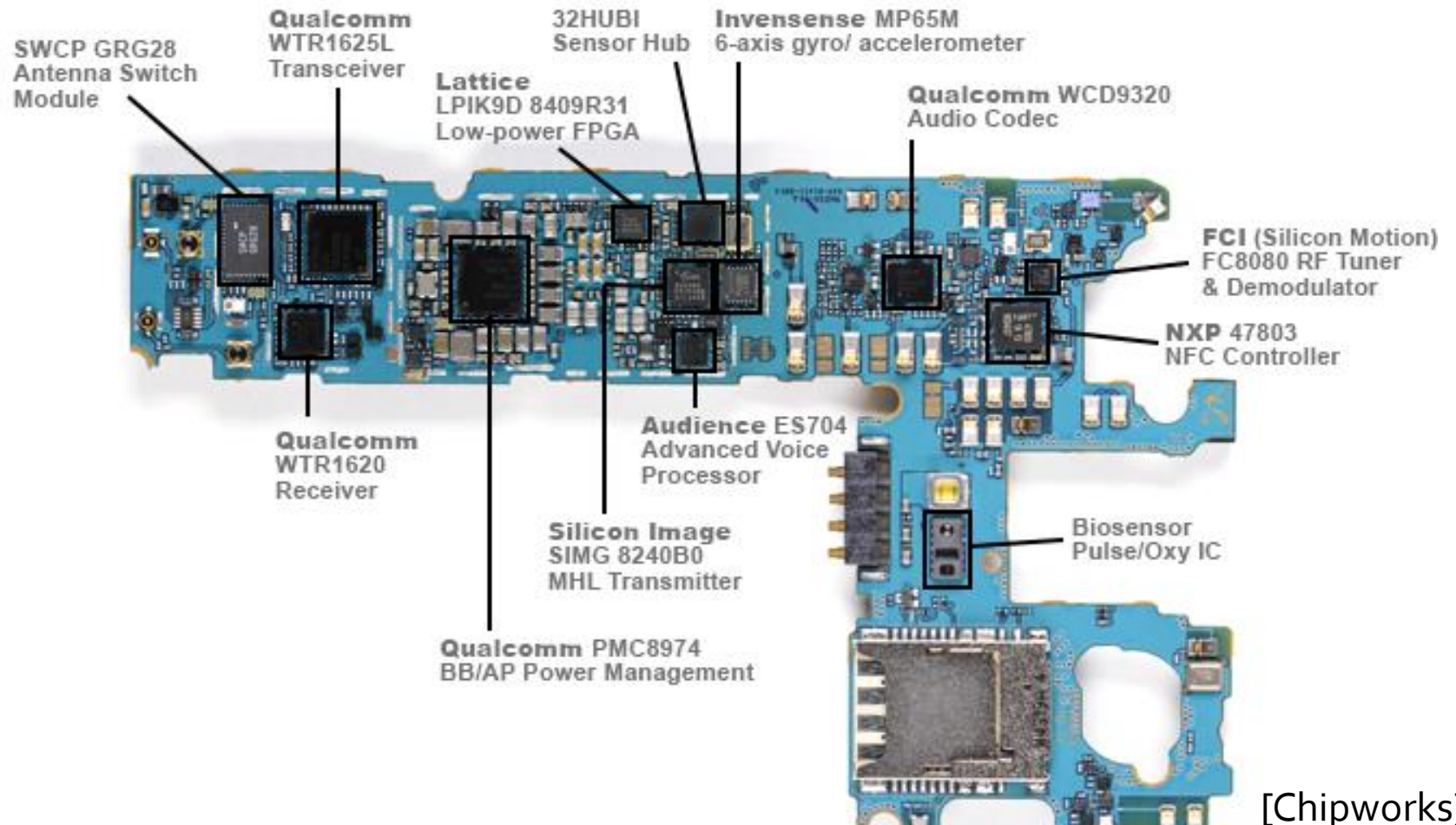
- ▶ Parts of the lecture notes are adopted from the previous works done by the members of Mixed-Signal IC and System Group (MICS) at SNU
: Hwanseok Yeo, Sigang Ryu, Seuk Son, Yoontaek Lee
- ▶ This work is enabled by the support of IDEC and Scientific Analog, Inc.

Cell-Based Design Flow for Mixed-Signal System

Jaeha Kim, Sung-Joon Lee, and Eunseo Kim
Mixed-Signal IC and System Group
Seoul National University
May 19. 2016

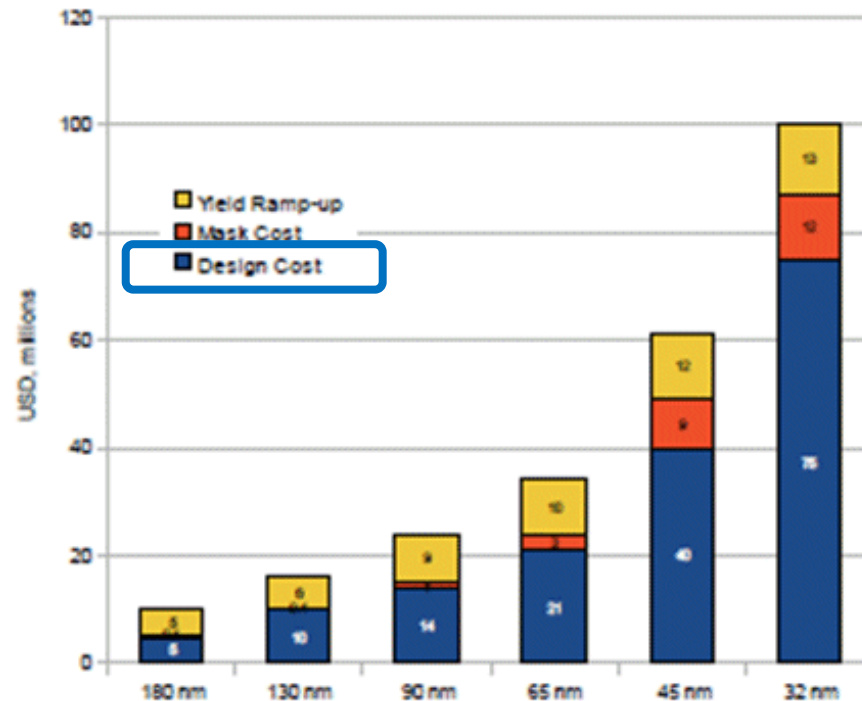
Demands on Analog Circuits

► Samsung Galaxy S5 teardown



IC Design Cost Skyrocketing

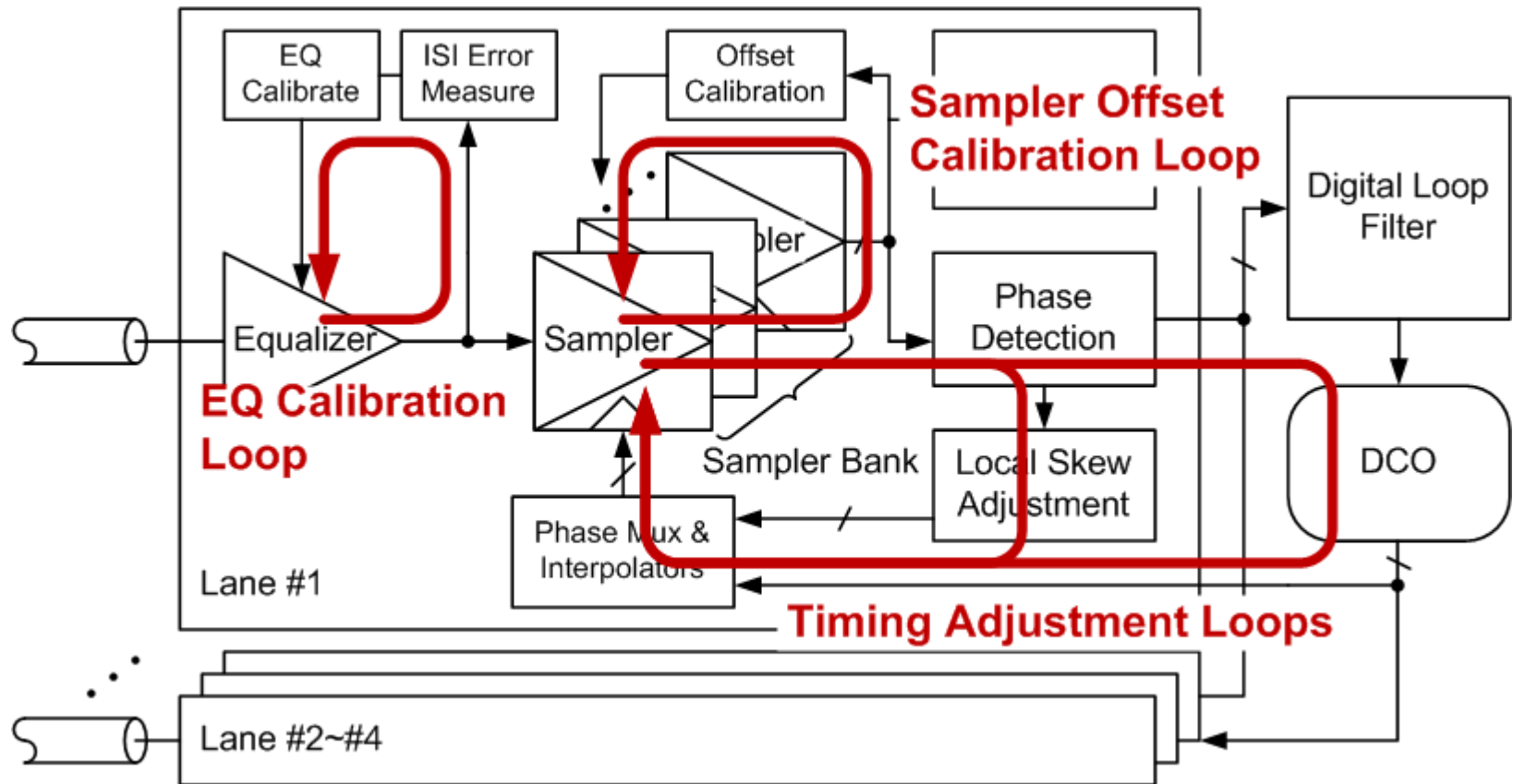
- ▶ With scaling of CMOS technology, design cost has been dramatically increased
- ▶ Due to rapid change in process, analog design is not able to catch the pace of digital design



[JRC, 2009]

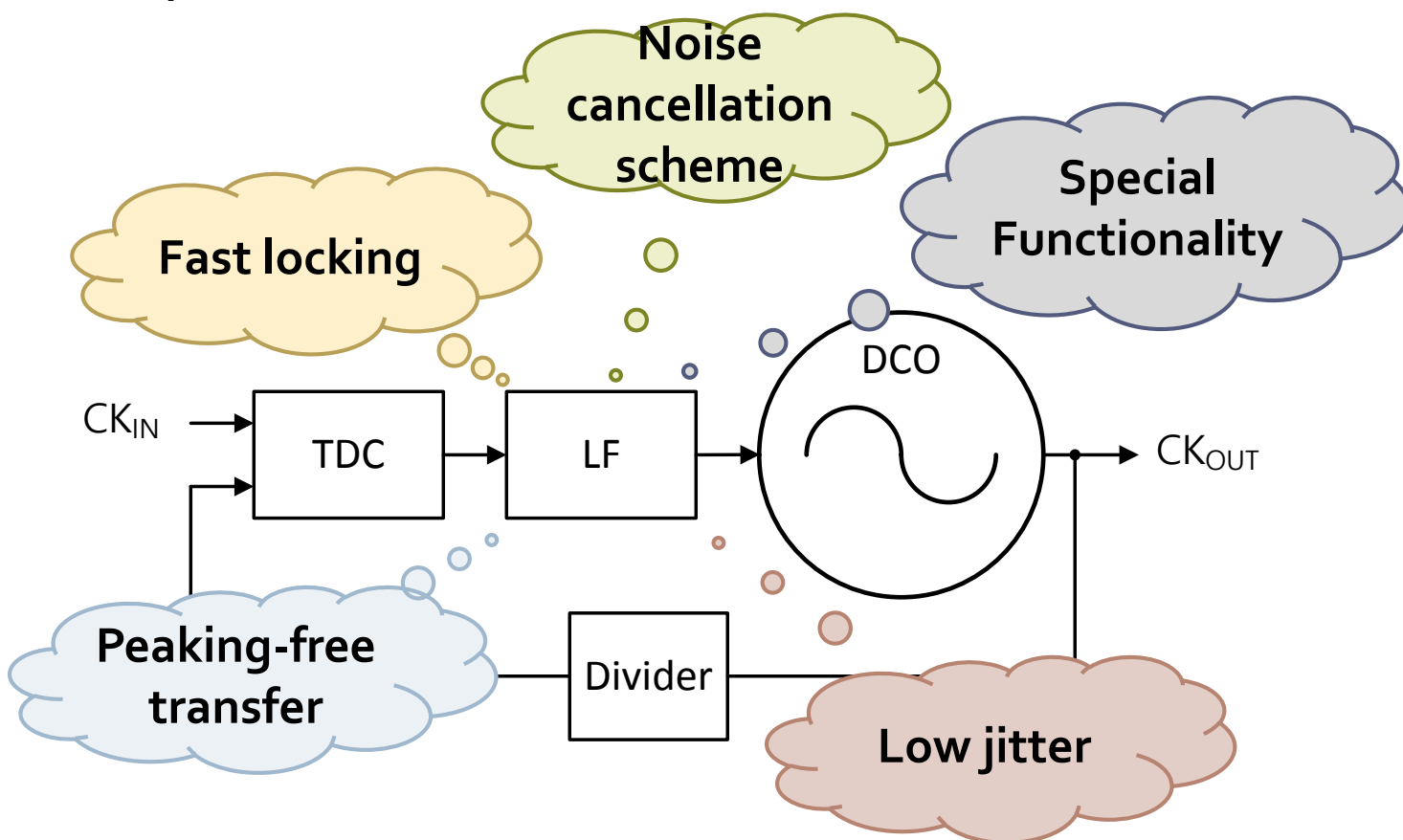
Challenge with Big D, Little A

- ▶ Today's mixed-signal systems are tightly coupled A+D
 - ▶ Calling for new methodologies for their design & verification



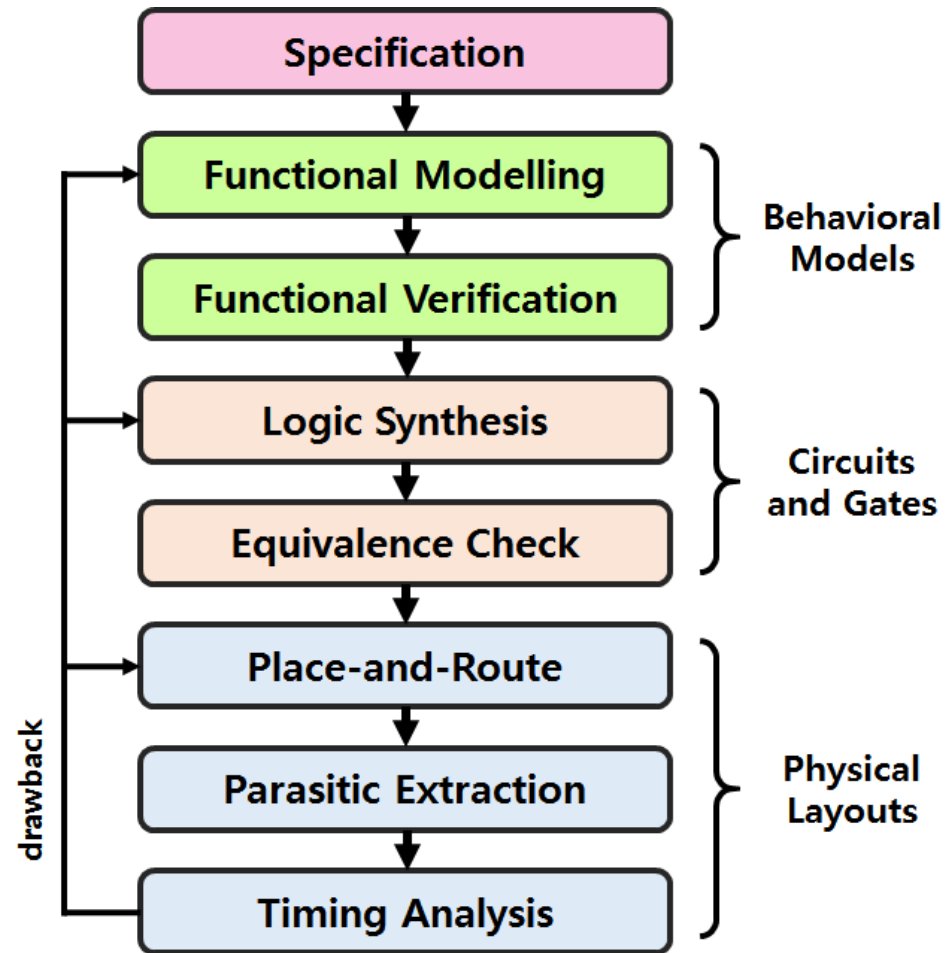
Popularity of Digital in Analog

- ▶ Designers employ large D in order to improve circuit system performance



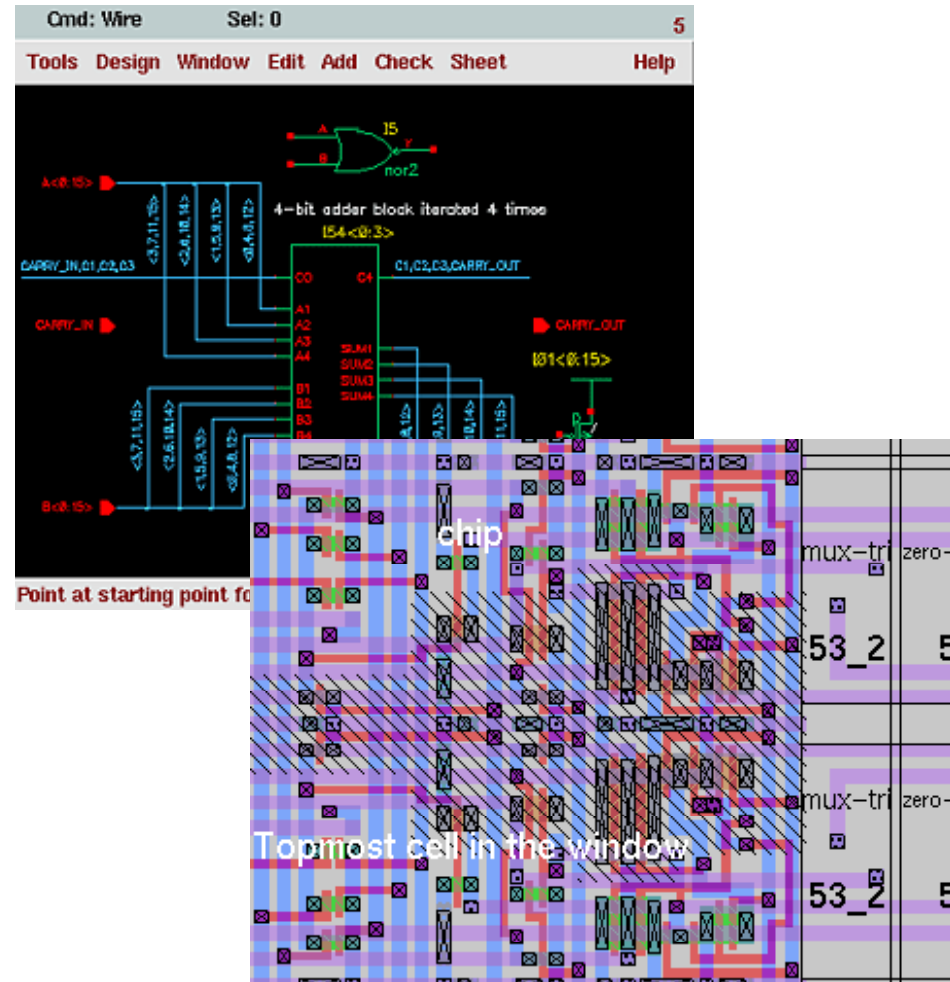
Digital Design is Systematic

- ▶ Digital flows starts by defining "***what we want***"
 - ▶ System-level functional modeling and verification
- ▶ Design is a process of mapping the intent into reality
 - ▶ The intent expressed in Boolean algebra



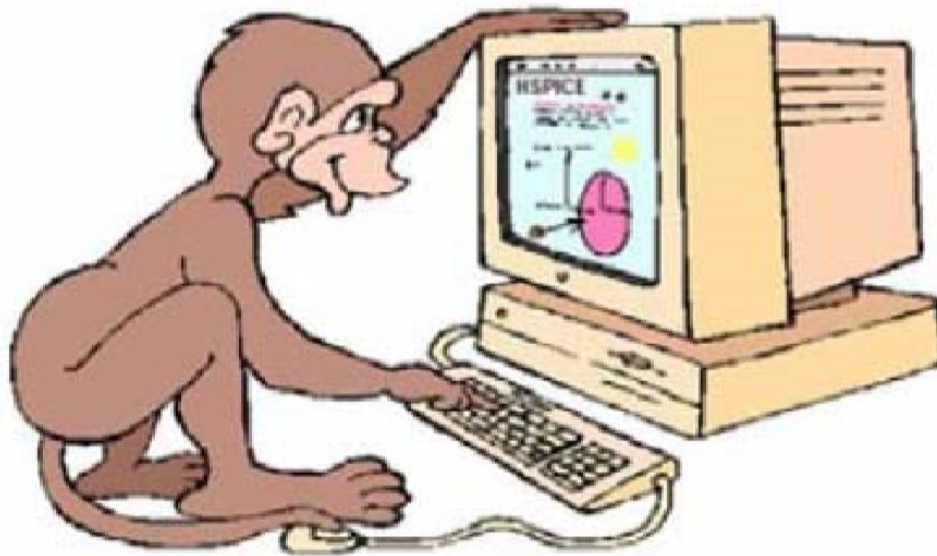
Analog Design is Manual

- ▶ Analog flows deal with “reality” from the start
 - ▶ Transistor-level circuit design
- ▶ Design is a process of scaling the components to a system
 - ▶ Largely manual
 - ▶ Lack of abstraction to aid scaling



Slow Analog Design Process

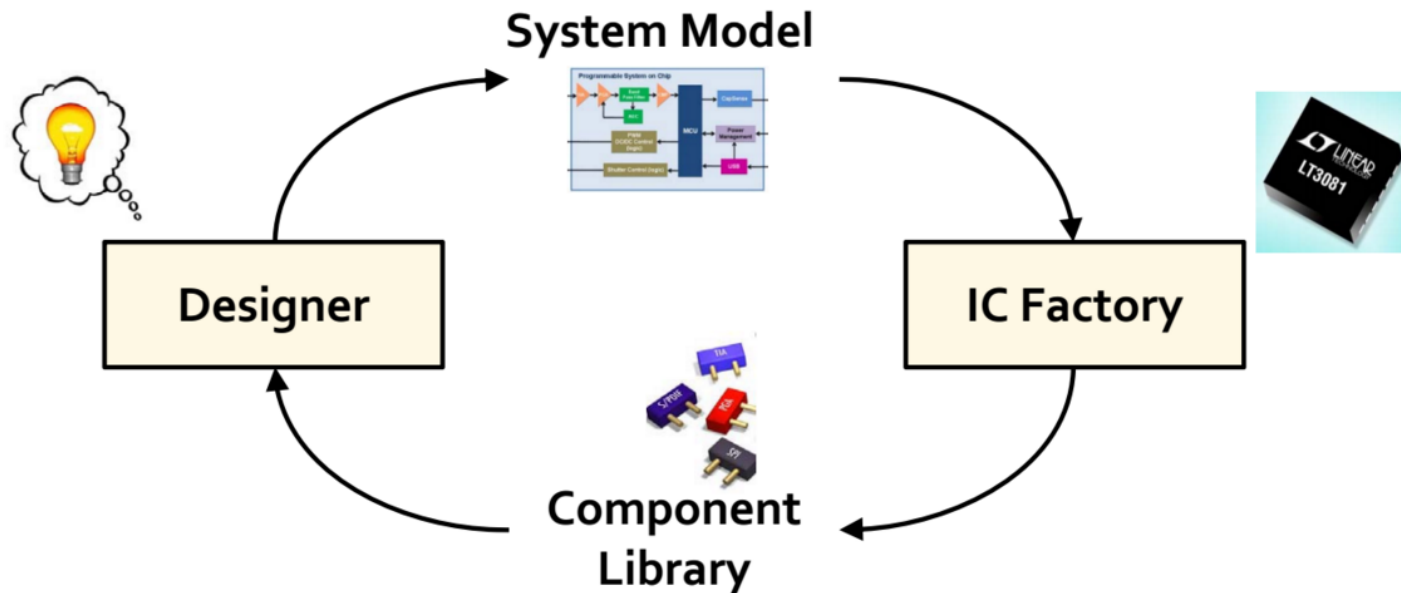
- ▶ Analog design is still largely based on manual efforts and human intuition/experience



[Courtesy: Isaac Martinez]

Change the Analog Design Flows

Can we design analog circuits just by putting together blocks?

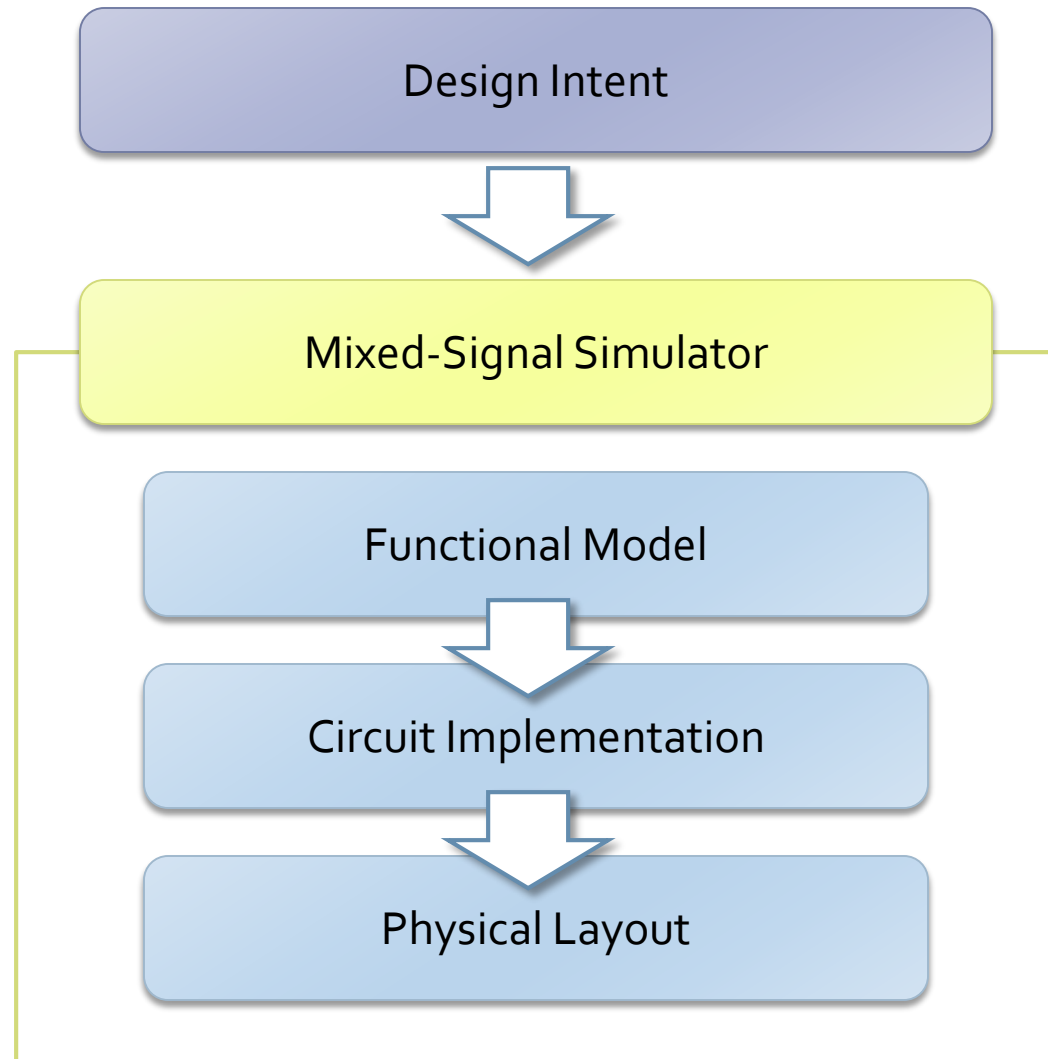


*With Cell-Based Design Flow, **YES!***

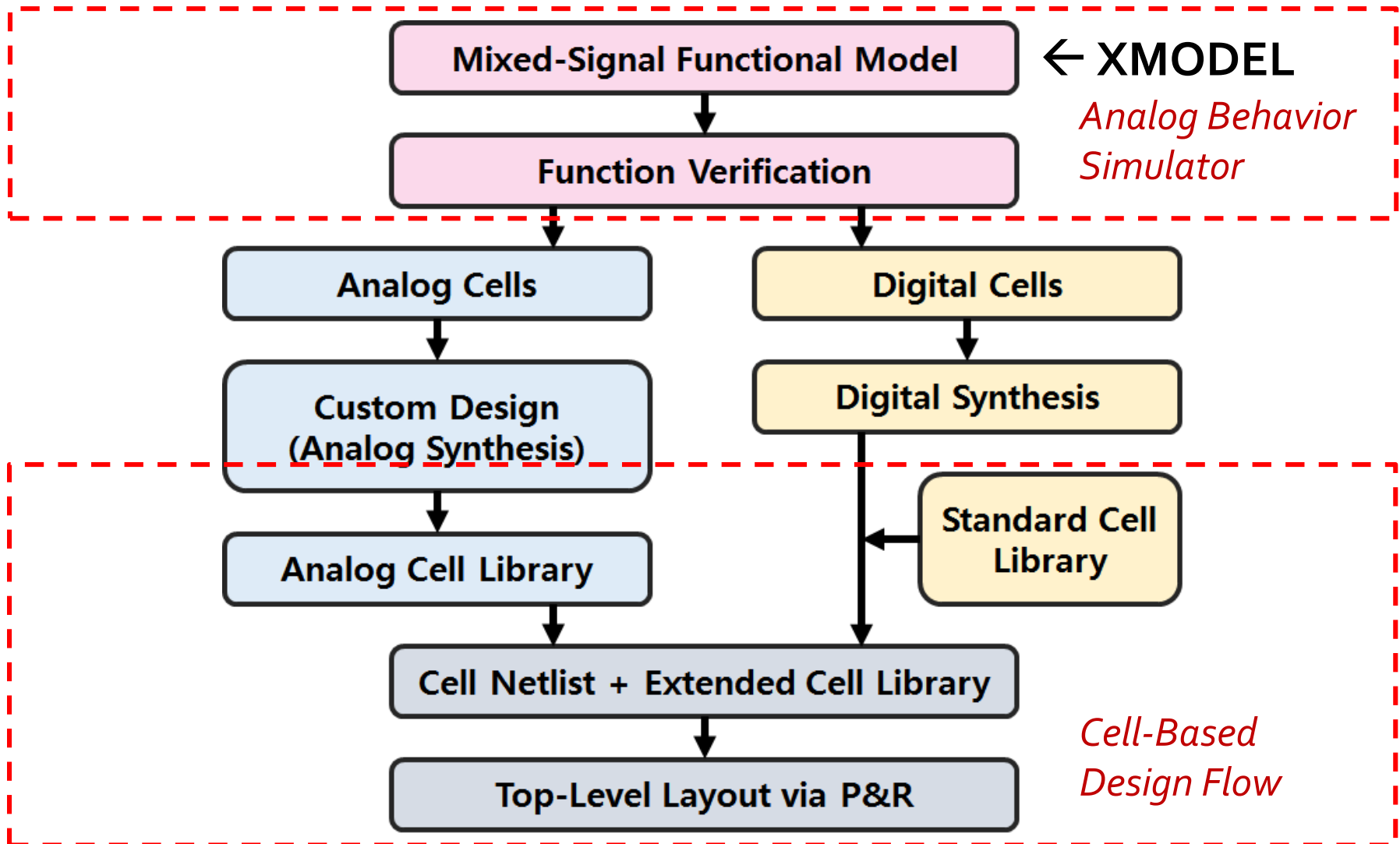
Concept of Cell-Based Design Flow

Systematic design flow

- ▶ Starting the design by verifying the functionality of the system model
- ▶ And then turning it into circuits and layout
- ▶ XMODEL can enable this top-down design flow!



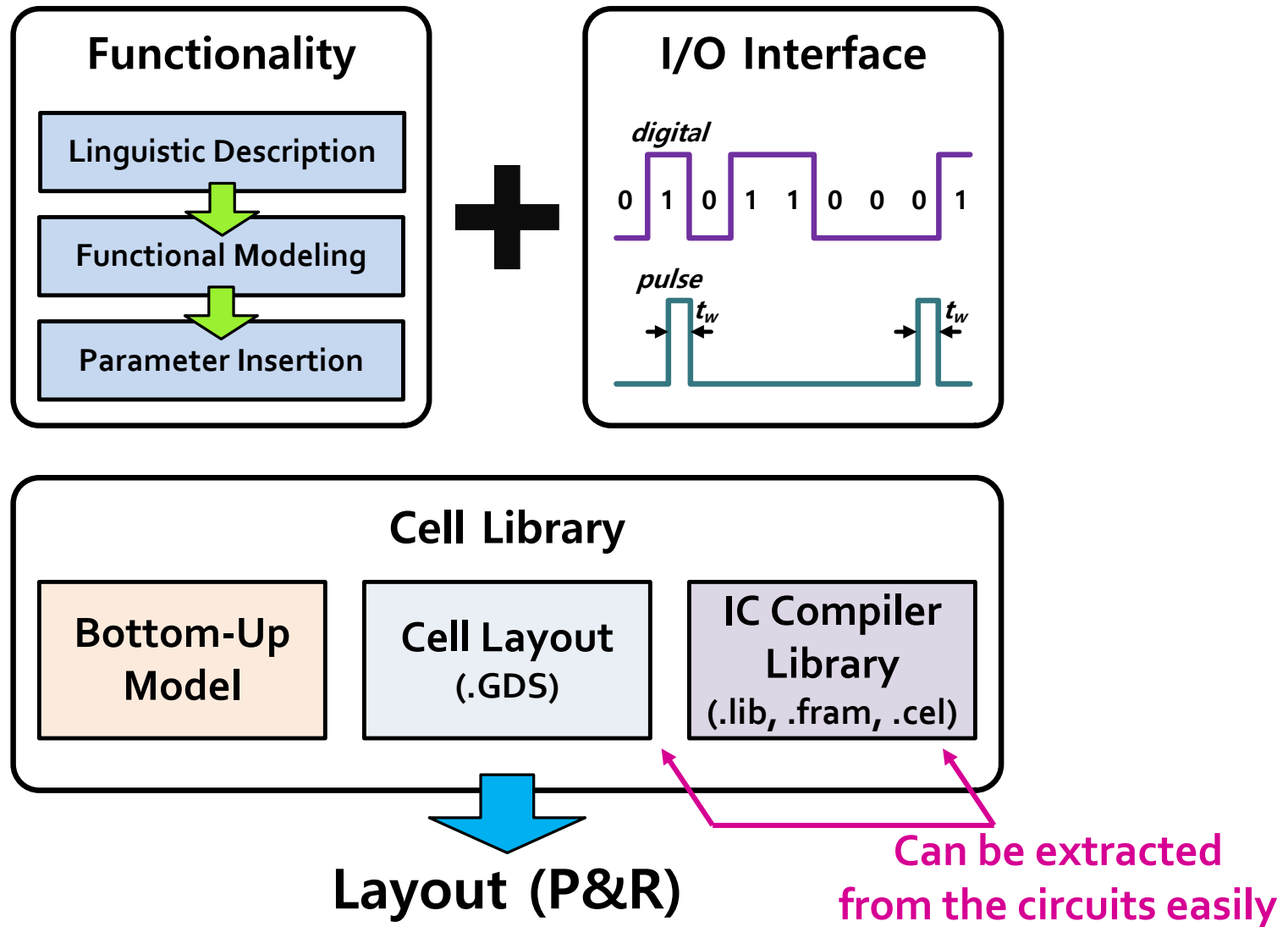
Cell-Based Design Flow for A/MS IC



Cell-Based Design Flow is Systematic

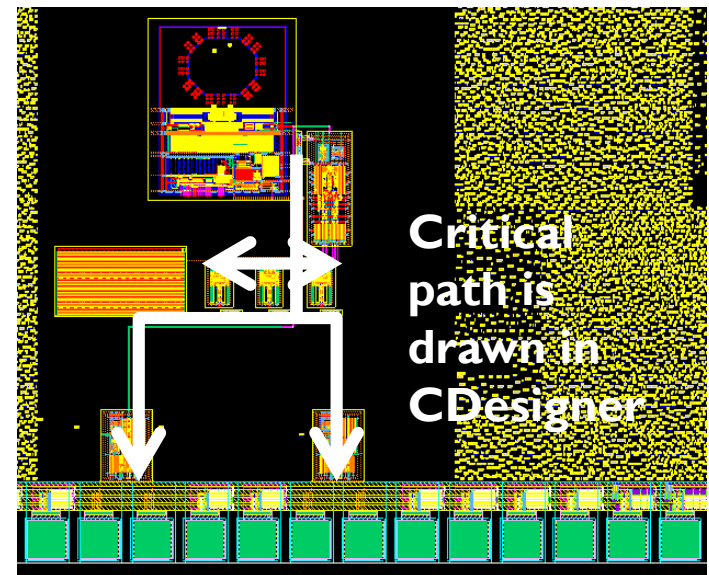
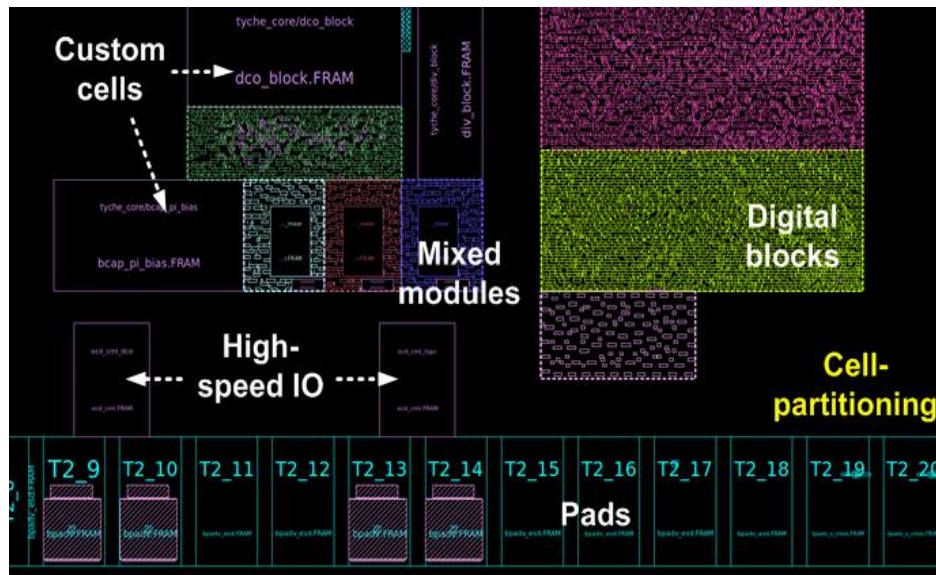
- ▶ **Model-first design flow**
- ▶ **Auto place & route for whole chip**
- ▶ **No manual routing at chip-level**

Cell Library Composition



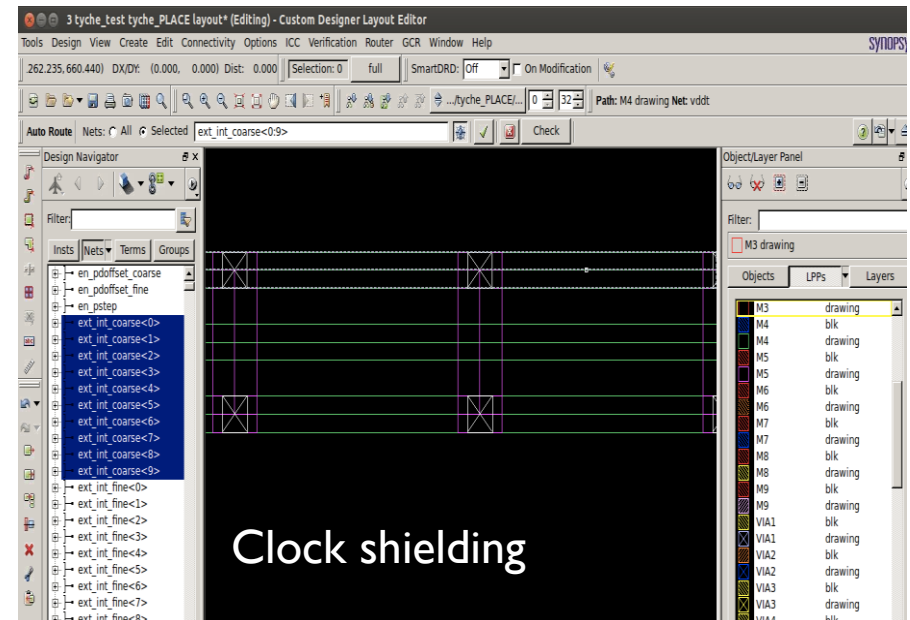
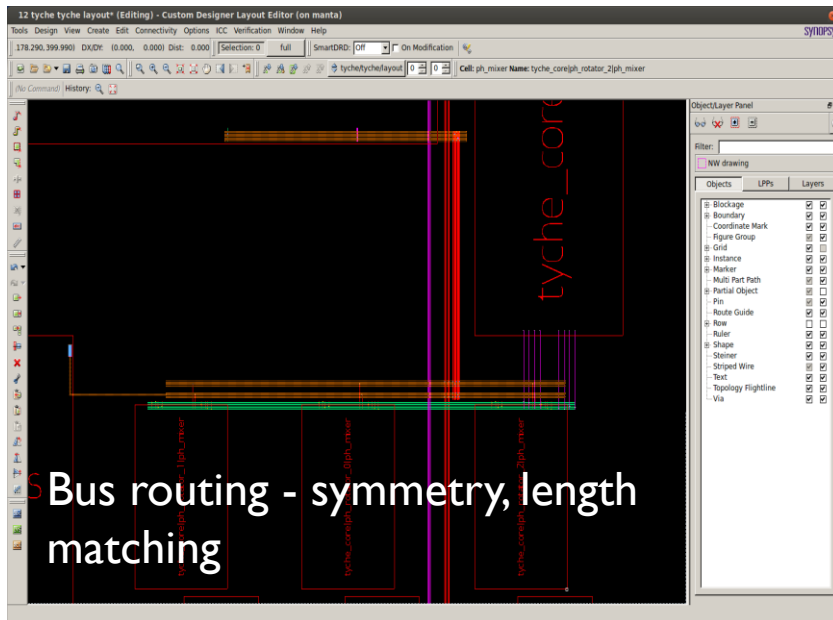
Pre-Placement & Pre-Routing using Custom Designer

- ▶ Critical analog cells can be pre-placed according to floorplan
- ▶ Critical signals such as high-speed, multi-phase clocks and analog bias signals can be pre-routed



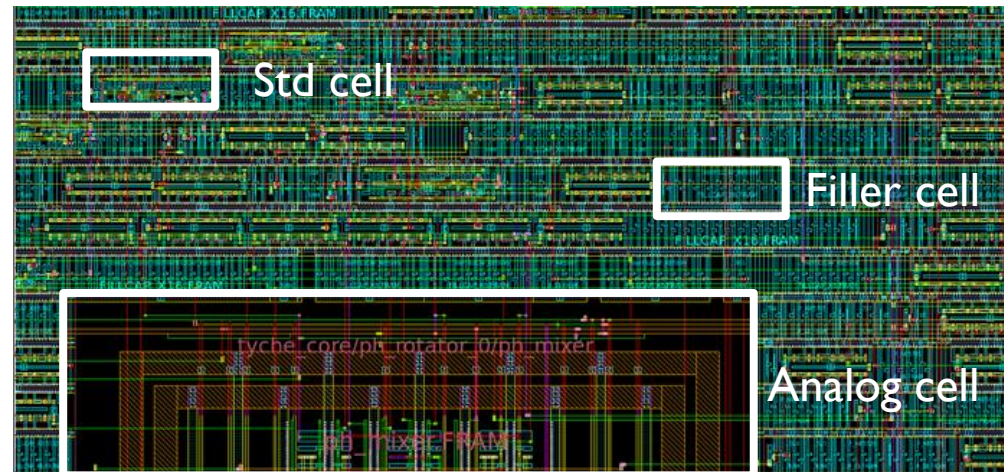
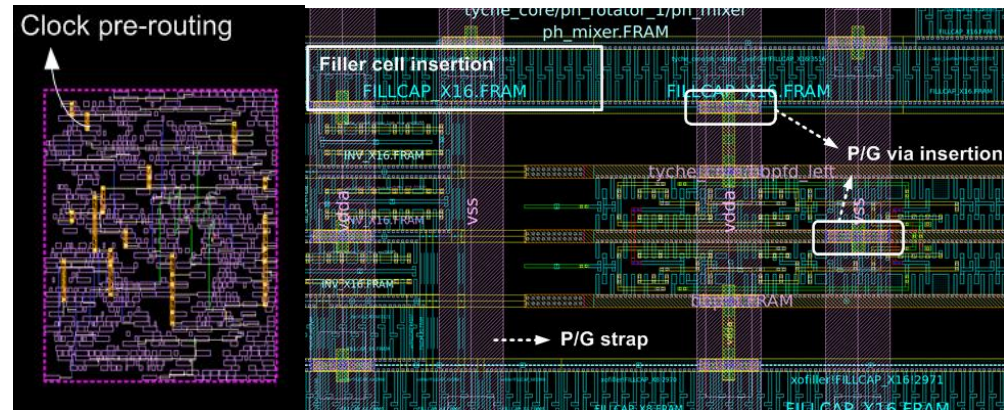
Pre-Routing in Custom Designer

- ▶ CD supports “AUTO ROUTE” that can automatically route wires according to analog constraints
 - ▶ Tools > Galaxy Custom Router (GCR) > Auto Route
 - ▶ Symmetry, length-matching, shielding, etc...
 - ▶ Repetitive patterns can be easily managed by Multi-Part Path



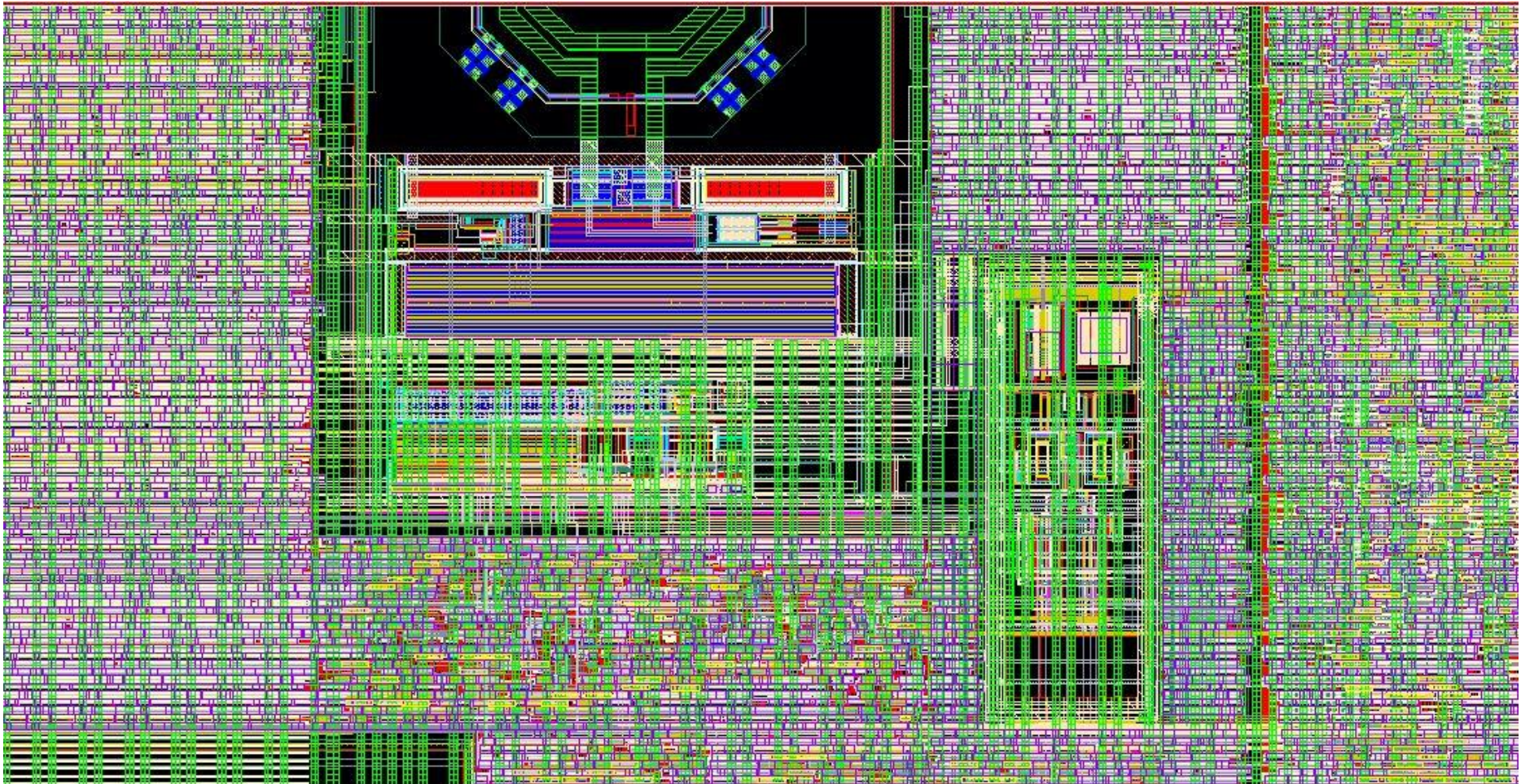
Place and Route in IC Compiler

- ▶ Synopsys IC Compiler can perform P&R on the rest of the cells and signals
 - ▶ Detail P&R
 - ▶ Buffer insertion
 - ▶ Power and ground routing
 - ▶ Via insertion
 - ▶ Clock-tree synthesis
 - ▶ Filler insertion
 - ▶ Antenna fix



Layout After P&R

► Digital + Analog + Clock Tree + Buffer + Filler + Routing

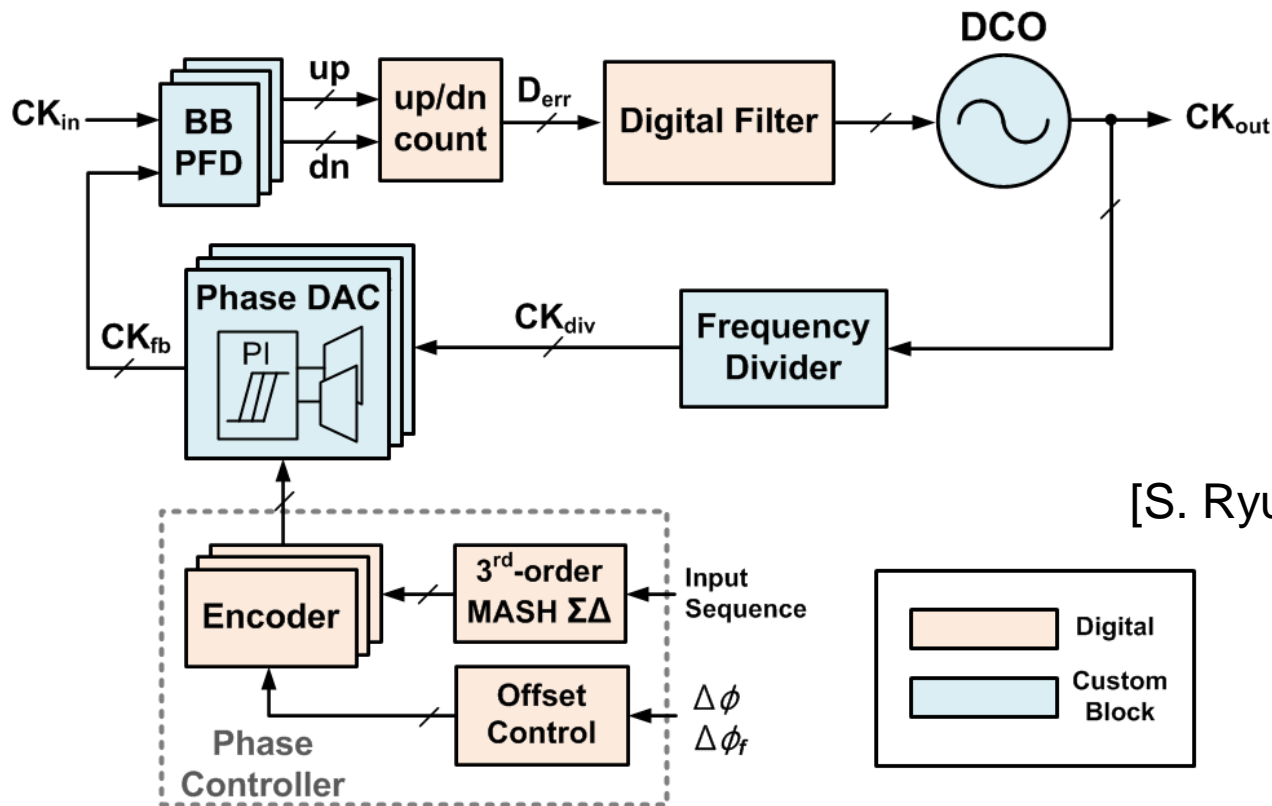


Example

(fabricated chips using cell-based design flow)

Example1: Digital Phase-Locked Loop

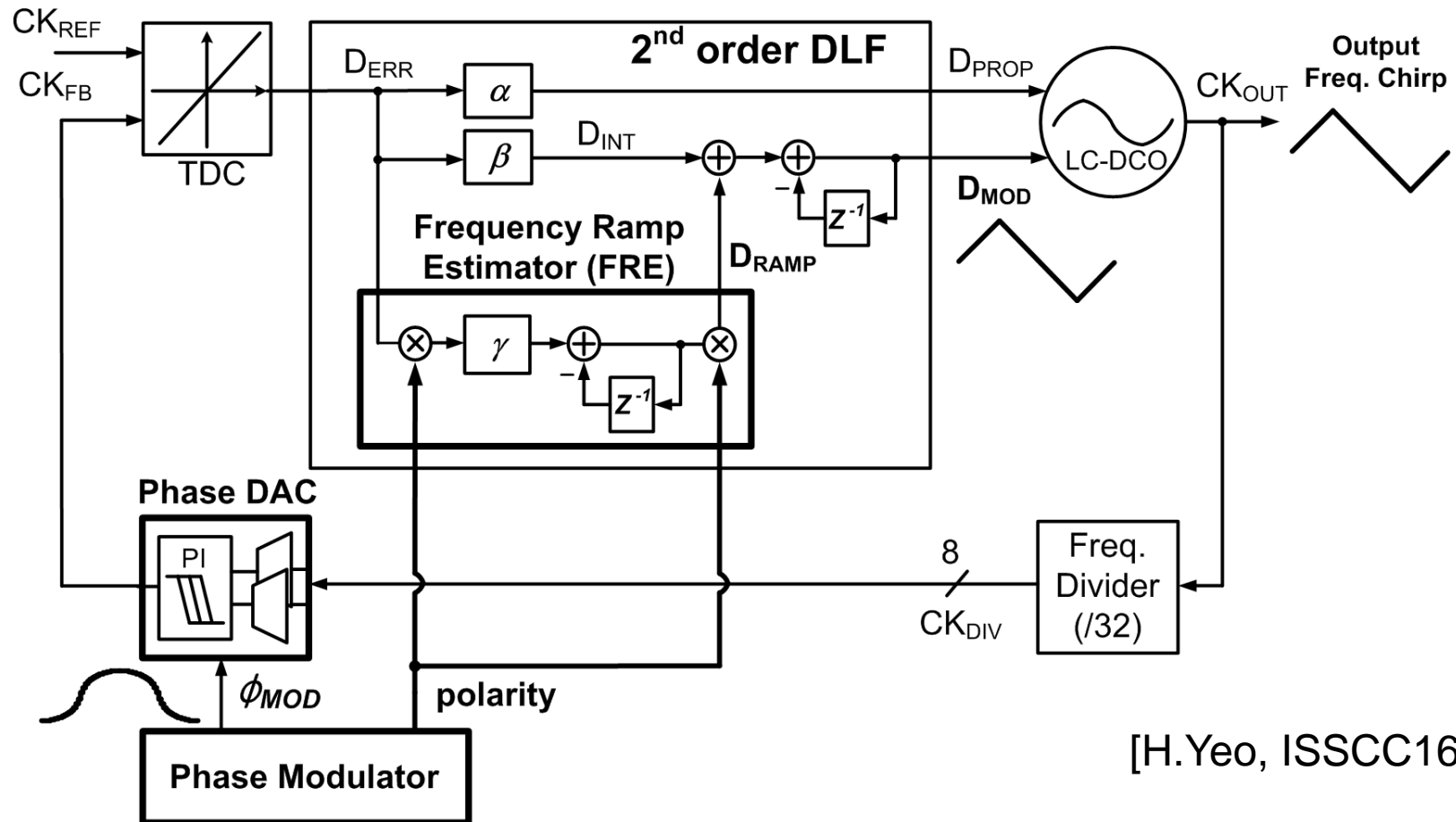
- ▶ 9.2-GHz digital PLL with peaking-free transfer function
 - ▶ The system is partitioned into analog/custom and digital blocks



[S. Ryu, JSSC14]

Example2: Fast Chirp Freq. Synthesizer

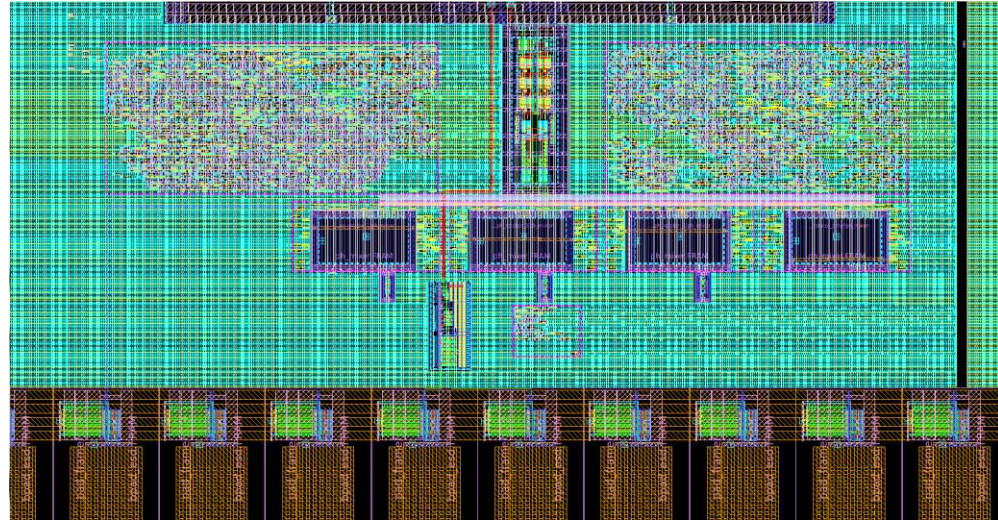
- ▶ A 940MHz-Bandwidth 28.8 μ s-Period 8.9GHz Chirp Frequency Synthesizer PLL



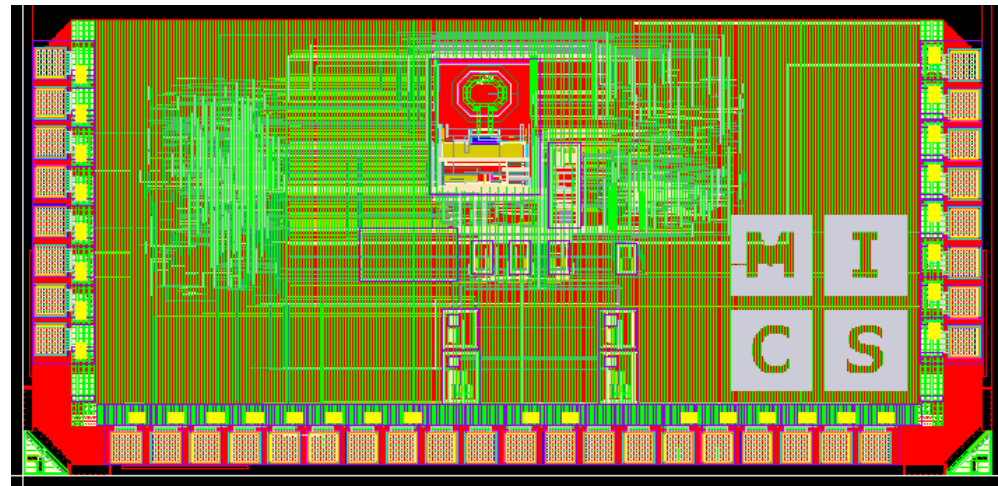
[H.Yeo, ISSCC16]

Finalized Chip After P&R

- ▶ Layout and die photograph of the prototype digital PLL
- ▶ The entire P&R process takes only 2~4 hours, enabling multiple iteration of the chip-level layout and validation for the run



[S. Ryu, JSSC14]

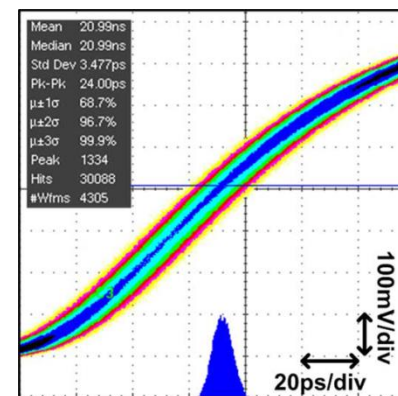
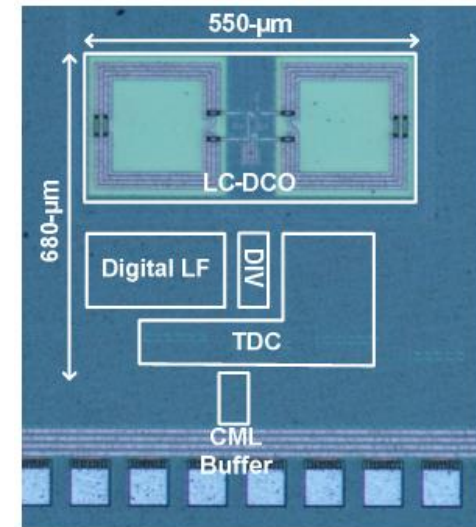


[H. Yeo, ISSCC16]

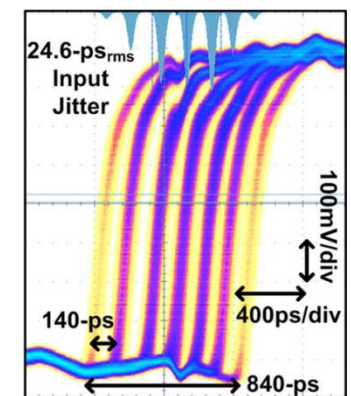
Die Photograph and Summary (Ex1)

- Demonstrates the feasibility of cell-based design flow

Property	Value
Technology	65nm 1P8M CMOS LP
Supply Voltage	1.2 V
Input Frequency	139 ~ 148.44 MHz
Output Frequency	8.9 ~ 9.5 GHz
Bandwidth	0.3 ~ 1.5 MHz
Clock Jitter (/8)	3.477 ps _{rms} at 1.15 GHz 24 ps _{pp}
Phase Noise	-93 dBc/Hz at 1MHz offset -115 dBc/Hz at 10MHz offset
Settling Time	1.58 μs at 0.69 MHz-BW
Power Dissipation	63.9 mW
Active Area	0.374 mm ²



(a)

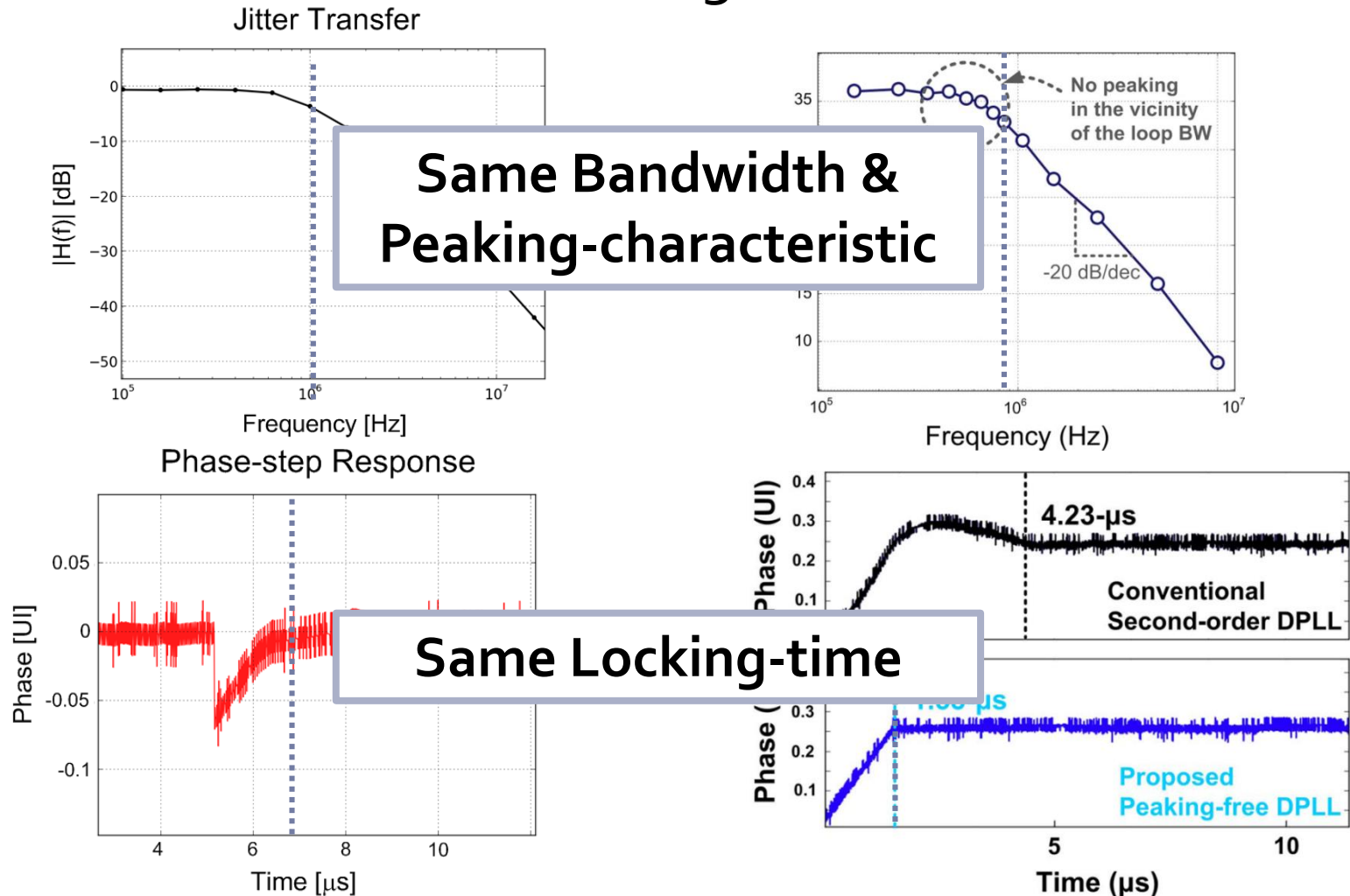


(b)

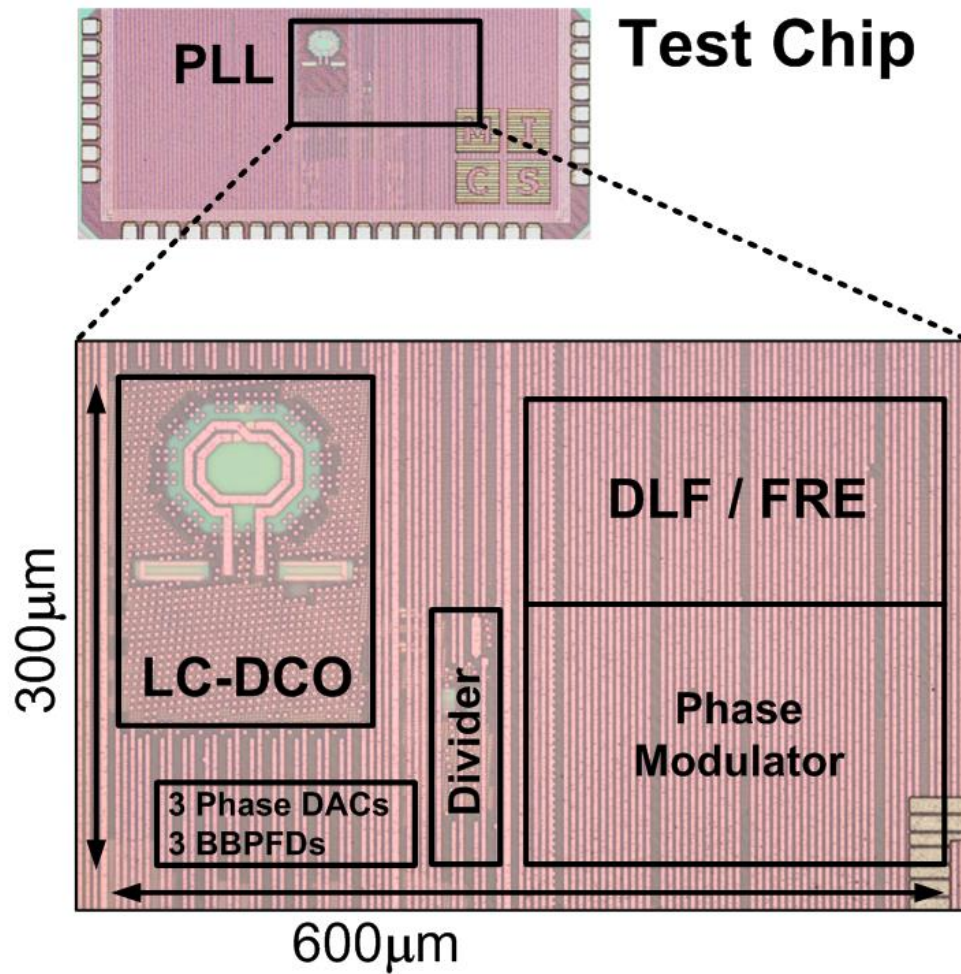
[S. Ryu, JSSC14]

Measurement Results (Ex1)

- ▶ The measurement results agree well with the simulation



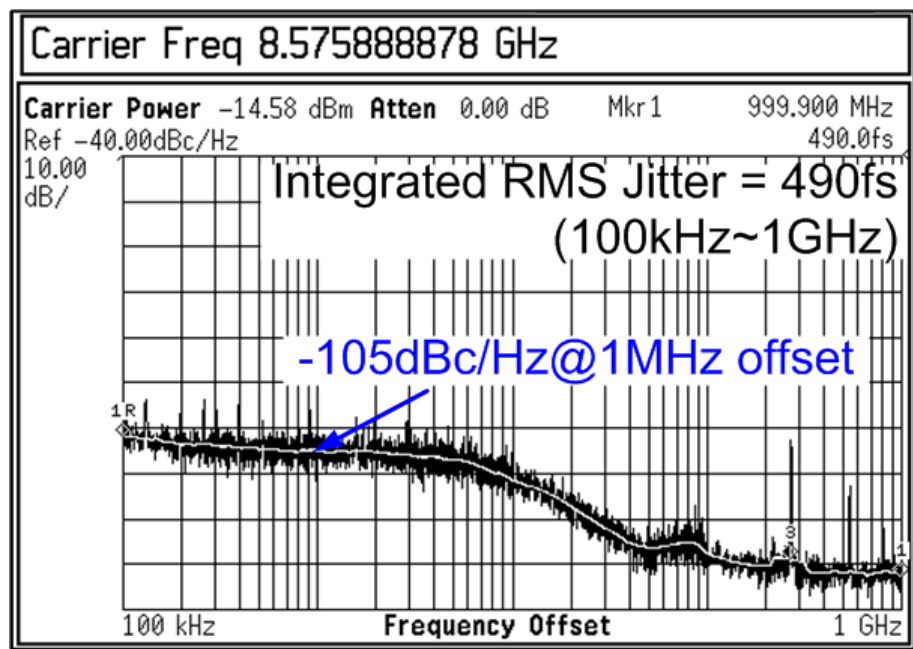
Die Photograph and Summary (Ex2)



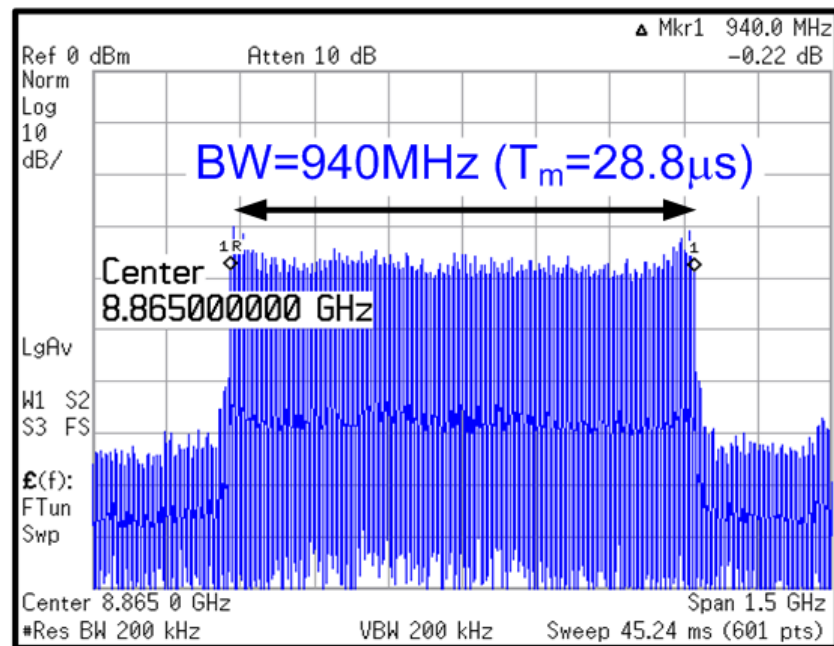
Technology	65nm 1P9M CMOS LP
Supply Voltage	1.1 ~ 1.3 V
Input Freq.	276.8 MHz
Output Freq.	8.4 ~ 9.4 GHz
Maximum Chirp Slope	32.63 MHz/μs
RMS Freq. Error	< 1.9 MHz (including turn-arounds)
Phase Noise (PLL)	-105.0 dBc/Hz @ 1MHz
Power Dissipation	14.8 mW
Active Area	0.18 mm ²

[H.Yeo, ISSCC16]

Measurement Results (Ex2)



Phase Noise (Without Chirp)



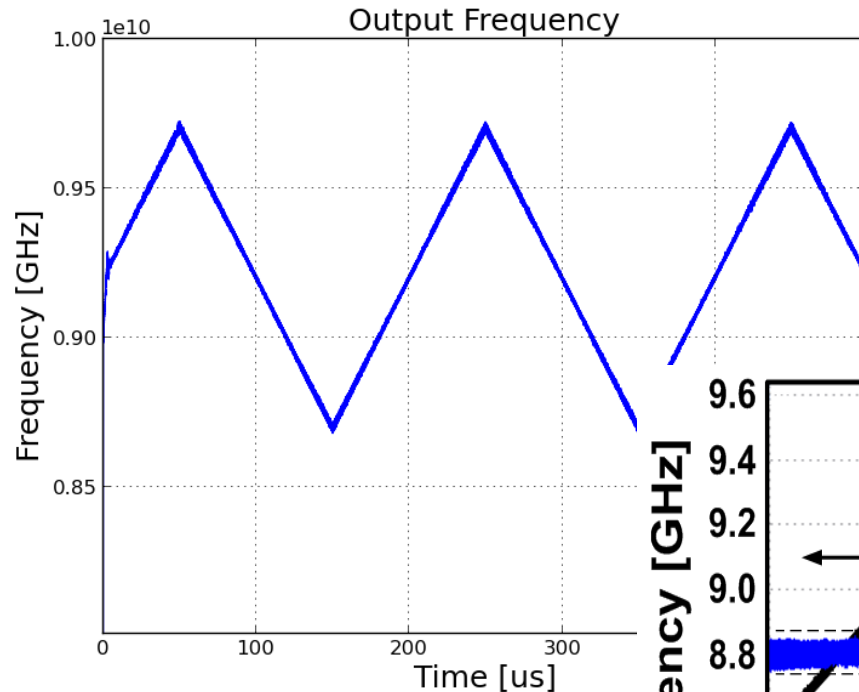
Power Spectrum (With Chirp)

[H.Yeo, ISSCC16]

- ▶ PLL phase noise without chirp
 - ▶ Integrated RMS jitter: **490fs_{rms}**
- ▶ Power spectrum with chirp

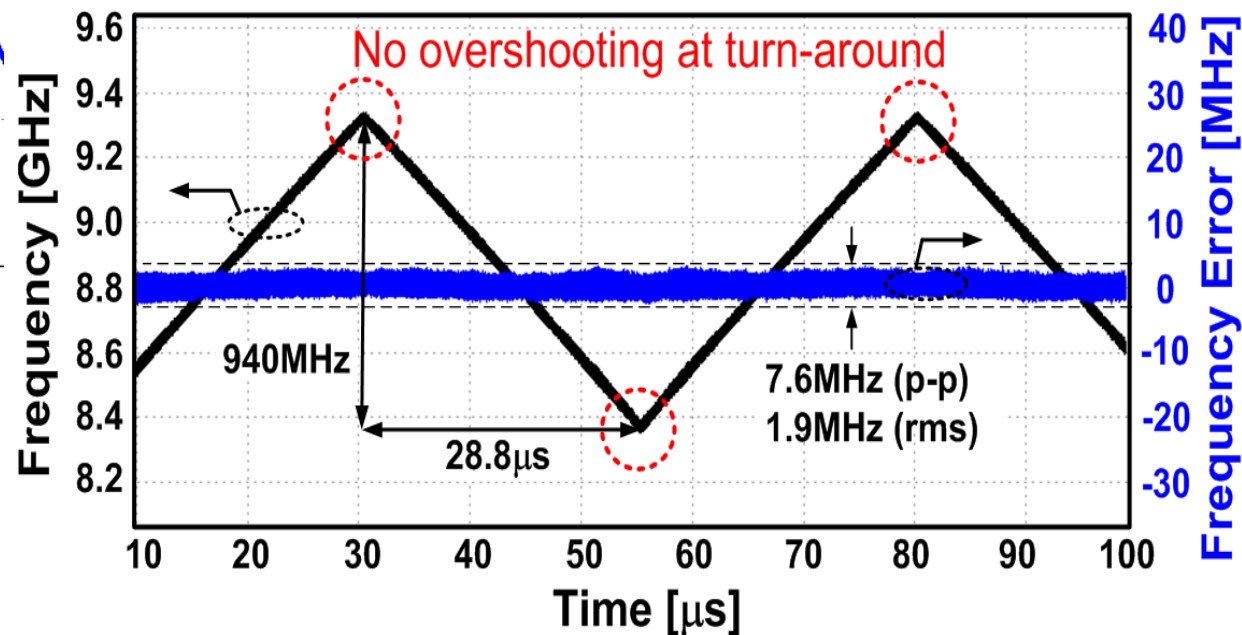
Measurement Results (Ex2)

- The measurement results agree well with the simulation



Measurement Result

Model-level Simulation Result



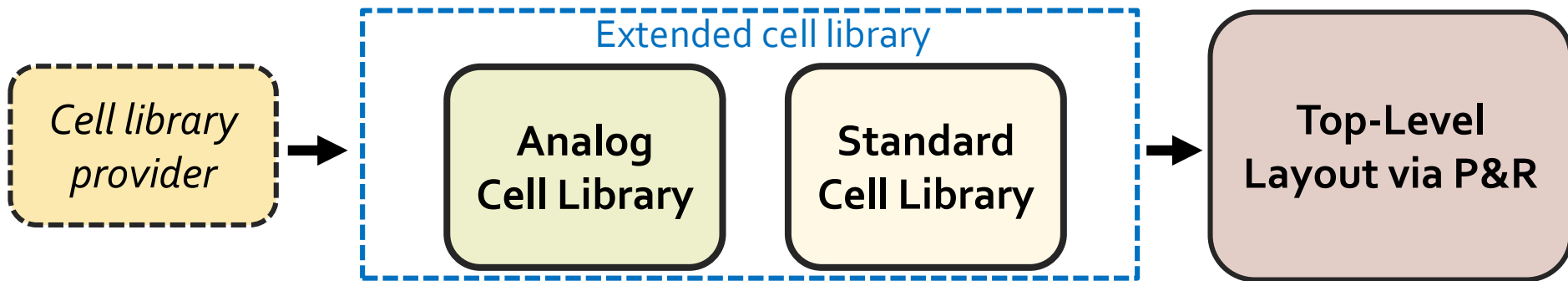
Summary

Summary

- ▶ Cell-based design flow
 - ▶ Model-first design flow
 - ▶ Auto place & route for whole chip
 - ▶ No manual routing in chip-level
- ▶ Block-level model and abstraction
 - ▶ Enabling circuit design just by cell libraries
- ▶ Digital Synthesis : Design Compiler
- ▶ Layout by P&R tools : IC Compiler / Custom Designer

Circuit Design Just by Cell Libraries

- ▶ A Circuit designer can make a chip **without the use of Cadence Virtuoso**



- ▶ Requirements for the analog cell library
 - 1) **Input/output interfaces** are well defined
 - 2) It should be represented by **definite functionality** (described by XMODEL)
 - 3) PVT robust circuit topology

Can Analog Circuit Design Become As Easy As Digital Design?

YES!